[NAME OF DOCUMENT] Abstract

[ABSTRACT]

[PURPOSE]

Providing a semiconductor device with a TFT structure with high reliability

[MEANS]

In a CMOS circuit formed on a substrate 100, a subordinate gate wiring line (a first wiring line) 102a and main gate wiring line (a second wiring line) 113a are provided in an n-channel TFT. The LDD regions 107a and 107b overlap the first wiring line 102a and not overlap the second wiring line 113a. Thus, applying a gate voltage to the first wiring line forms the GOLD structure, while not applying forms the LLD structure. In this way, the GOLD structure and the LLD structure can be used appropriately in accordance with the respective specifications required for the circuits.

[SELECTED FIGURE] Fig. 1